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Examiner Signature		Date Considered	
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application Number	09/838,678
				Filing Date	April 19, 2001
				First Named Inventor	Uhl, Augustus K.
				Art Unit	2183
				Examiner Name	O'BRIEN, BARRY J.
Sheet	2	of	8	Attorney Docket Number	022193-010310US

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
AL	1	Agerwala et al., "Data Flow Systems - Special Issue," <i>IEEE COMPUTER</i> , vol. 15, no. 2, pp. 10-13, 1982.		
AL	2	Aiken et al., "Perfect Pipelining: A New Loop Parallelization Technique," in <i>Proceedings of the 1988 European Symposium on Programming</i> , 1988, 15 pages total.		
AL	3	Austin et al., "Dynamic Dependency Analysis of Ordinary Programs," in <i>Proceedings of the 19th Annual International Symposium on Computer Architecture, Gold Coast, Australia</i> , pp. 342-351, IEEE and ACM, May 1992.		
AL	4	Banerjee et al., "Fast Execution of Loops With IF Statements," <i>IEEE Transactions on Computers</i> , vol. C-33, pp. 1030-1033, November 1984.		
AL	5	Beck et al., "The cydra 5 minisupercomputer: Architecture and implementation," <i>Journal of Supercomputing</i> , vol. 7, pp. 143-180, 1993.		
AL	6	Brekelbaum et al., "Hierarchical Scheduling Windows," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> . Istanbul, Turkey: IEEE, ACM, November 2002.		
AL	7	Burger et al., "Billion-Transistor Architectures," <i>IEEE COMPUTER</i> , vol. 30, no. 9, September 1997.		
AL	8	Burger et al., "The SimpleScalar Tool Set, Version 2," URL: http://www.simplescalar.com/docs/users_guide_v2.pdf , created 1997, accessed: June 14, 2002.		
AL	9	Calder et al., "Value profiling," in <i>Proceedings of the 30th IEEE Symposium on Microarchitecture</i> , December 1997.		
AL	10	Chen, "Supporting Highly Speculative Execution via Adaptive Branch Trees," in <i>Proceedings of the 4th Annual International Symposium on High Performance Computer Architecture</i> : IEEE, January 1998, pp. 185-194.		
AL	11	Cleary et al., "Scaling the reorder buffer to 10,000 instructions," in <i>IEEE TCCA News</i> , pp. 16-20, June 2000.		
AL	12	Cleary et al., "The Architecture of an Optimistic CPU: The Warp Engine," in <i>Proceedings of the HICSS95</i> , pp.163-172, University of Hawaii, January 1995.		
AL	13	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler," <i>IEEE Transactions on Computers</i> , vol. C-37, pp. 967-979, August 1988.		
AL	14	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," in <i>Proceedings of the Second International Conference Architectural Support for Programming Languages and Operating Systems (ASP LOS II)</i> : ACM and IEEE, September 1987, pp. 180-192.		
AL	15	Cragon, <i>Branch Strategy Taxonomy and Performance Models</i> , Los Alamitos, California: IEEE Computer Society Press, 1992, 9 pages total.		
AL	16	Cytron, "Doacross: Beyond Vectorization for Multiprocessors (Extended Abstract)," in <i>Proceedings of the 1986 International Conference on Parallel Processing</i> , pp. 836-844, Pennsylvania State University and the IEEE Computer Society, August 1986.		
Examiner Signature	Amee Li		Date Considered	6-23-2005

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AL	17	Dutta et al., "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," in <i>Proceedings of the 28th International Symposium on Microarchitecture (MICRO-28)</i> , pp. 258-263, IEEE and ACM, November/December 1995.	
AL	18	Ebcioğlu et al., "DAISY: Dynamic Compilation for 100% Architectural Compatibility," IBM Research Report RC 20538, IBM Research Division, August 5, 1996, 82 pages total.	
AL	19	Ebcioğlu, "A Compilation Technique for Software Pipelining of Loops with Conditional Jumps," in <i>Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO20)</i> , pp. 69-79, Association of Computing Machinery, December 1987	
AL	20	Ellis, <i>Bulldog: A Compiler for VLIW Architectures</i> . PhD thesis, Yale University, New Haven, CT, 292 total pages, 1985.	
AL	21	Foster et al., "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Transactions on Computers</i> , vol. C-21, pp. 1411-1415, December 1972.	
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AL	23	Franklin et al., "The Expandable Split Window Paradigm for Exploiting Fine-Grain Parallelism," in <i>Proceedings of the 19th International Symposium on Computer Architecture</i> , pp. 58-67, ACM, May 1992.	
AL	24	Ginosar et al., "Adaptive Synchronization," in <i>Proceedings of the 1998 International Conference on Computer Design</i> , 2 pages total, 1998.	
AL	25	Glass, "Crusoe: Transmeta comes out of the closet," in http://www.linuxplanet.com/linuxplanet/reports/1441/1/ , 6 pages total, 2000.	
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AL	27	Gopal et al., "Speculative Versioning Cache," University of Wisconsin, Madison, Technical Report TR-1334, 11 pages total, July 1997.	
AL	28	Gostelow, "The u-interpreter," <i>IEEE Computer</i> , vol. 15, pp. 42-49, February 1982.	
AL	29	Gurd et al., "The manchester prototype dataflow computer," <i>Communications of the ACM</i> , vol. 28, pp. 34-52, January 1985.	
AL	30	Henning, "SPEC CPU2000: Measuring CPU Performance in the New Millennium," <i>IEEE COMPUTER</i> , vol. 33, no. 7, pp. 28-35, July 2000.	
AL	31	Henry et al., "Circuits for Wide-Window Superscalar Processors," in <i>Proceedings of the 27th Annual International Symposium on Computer Architecture</i> . Vancouver, BC, Canada: IEEE and ACM, June 10-14, 2000, pp. 236-247.	
AL	32	Henry et al., "The Ultrascalar Processor: An Asymptotically Scalable Superscalar Microarchitecture," in <i>HIPC '98</i> , December 1998, URL: http://ee.yale.edu/papers/HIPC98-abstract.ps.gz , 18 pages total.	

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AL	33	Huck et al., "Introducing the ia-64 architecture," in <i>IEEE Micro</i> , pp. 12-23, September 2000.		
AL	34	Jefferson, "Virtual Time," <i>Transactions on Programming Languages and Systems</i> , vol.7, no. 3, pp. 404-425, July 1985.		
AL	35	Jouppi et al., "Available instruction-level parallelism for superscalar and superpipelined machines," in <i>Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pp. 272-282, April 1989.		
AL	36	Karkhanis et al., "A Day in the Life of a Data Cache Miss," in <i>Proceedings of the 2nd Annual Workshop on Memory Performance Issues (WMPI)</i> , at the 29th International Symposium on Computer Architecture (ISCA 2002), Anchorage, Alaska, May 2002.		
AL	37	Khalafi et al., "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, Technical Report 032002-0101, April 2, 2002, URL: http://www.ele.uri.edu/~uht/papers/Levo4TR032002-01.01.pdf , 11 pages total.		
AL	38	Kim et al., "An Instruction Set Architecture and Microarchitecture for Instruction Level Distributed Processing," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , Anchorage, Alaska, USA: ACM, May 25-29, 2002.		
	39	Klauser et al., "Dynamic Hammock Predication for Non-predicated Instruction Set Architectures," in <i>Int'l. Conf on Parallel Architectures and Compilation Techniques (PACT)</i> , Paris, France, October 1998, pp. 278-285.		
	40	Krewell, "IntelQ01 Earnings Plummet," <i>Cahners Microprocessor</i> , vol. 15, no. 5, May 2001, 1 page total.		
AL	41	Krewell, "Intel's McKinley Comes Into View," <i>Cahners Microprocessor</i> , vol. 15, no. 10, pp. 1,5 October 2001.		
AL	42	Kumar, "Measuring Parallelism in Computation-Intensive Scientific/Engineering Applications," <i>IEEE Transactions on Computers</i> , vol. 37, no. 9, pp. 1088-1098, September 1988.		
AL	43	Lam et al., "Limits of Control Flow on Parallelism," in <i>Proceedings of the 19th Annual International Symposium on Computer Architecture</i> , Gold Coast, Australia: IEEE and ACM, May 1992, pp. 46-57.		
AL	44	Lebeck et al., "A Large, Fast Instruction Window for Tolerating Cache Misses," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , Anchorage, Alaska, USA: ACM, May 25-29, 2002, 12 pages total.		
AL	45	Lee et al., "Branch Prediction Strategies and Branch Target Buffer Design," <i>COMPUTER</i> , vol. 17, pp. 6-22, January 1984.		
AL	46	Lepak et al., "On the value locality of store instructions," in <i>Proceedings of the International Symposium on Computer Architecture</i> , pp. 182-191, June 2000.		
AL	47	Lilja, "Reducing the Branch Penalty in Pipelined Processors," <i>COMPUTER</i> , vol. 21, pp. 47-55, July 1988.		

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AL	48	Lipasti et al., "Superspeculative Microarchitecture for Beyond AD 2000," <i>IEEE COMPUTER</i> , vol. 30, no. 9, pp. 59-66, September 1997.	
AL	49	Lipasti et al., "Value Locality and Load Value Prediction," in <i>Proceedings of the Seventh Annual International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS- VII)</i> . Boston, MA: IEEE and ACM, October 1996, pp. 138-147.	
AL	50	Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors," in <i>Proceedings of the 22nd Annual International Symposium on Computer Architecture</i> , pp. 138-149, IEEE and ACM, May 1995.	
	51	Martin et al., "Timestamp snooping: An approach for extending smps," in <i>Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pp. 25-36, November 2000.	
AL	52	Morano et al., "Implications of Register and Memory Temporal Locality for Distributed Microarchitectures," Dept. of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA, Technical Report, October 2002, pp 1-20, URL: http://www.ece.neu.edu/groups/nucar/publications/interval_ls.pdf	
AL	53	Morano et al., "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," in <i>Proceedings of the Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues (MEDEA 2002)</i> , at PACT 2002, Charlottesville, Virginia, USA, September 22, 2002, pp 16-25. Also appears in ACM SIGARCH Computer Architecture Newsletter, March 2003, URL: http://www.ele.uri.edu/~uht/papers/MEDEA2002final.pdf .	
AL	54	Morano, "Execution-Time Instruction Predication," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881, Technical Report 0320020100, March 2002, pp. 1-10, URL: http://www.ele.uri.edu/~uht/papers/Lavo3TR032002-0100.pdf .	
AL	55	Nagarajan et al., "A Design Space Evaluation of Grid Processor Architectures," in <i>Proceedings of the 30th Annual ACM/IEEE International Symposium on Microarchitecture</i> . Austin, Texas, USA: ACM, December 2001, pp. 40-51.	
AL	56	Pajuelo et al., "Speculative Dynamic Vectorization," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> . Anchorage, Alaska, USA: ACM, May 25-29, 2002.	
AL	57	Papworth, "Tuning the Pentium Pro Microarchitecture," <i>IEEE MICRO</i> , vol. 16, no. 2, pp. 8-15, April 1996.	
AL	58	Parcerisa et al., "Efficient Interconnects for Clustered Microarchitectures," in <i>Proceedings of the Eleventh International Conference on Parallel Architectures and Compilation Techniques</i> . Charlottesville, Virginia, USA: IEEE, September 22-25, 2002 10 pages total.	
AL	59	Park et al., "Reducing Register Ports for Higher Speed and Lower Energy," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> . Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
AL	60	Patt et al., "HPS, a New Microarchitecture: Rationale and Introduction," in <i>Proceedings of the Eighteenth Annual Workshop on Microprogramming (MICRO-18)</i> : IEEE and ACM, December 1985, pp. 103-108.	
AL	61	Popescu et al., "The Metaflow Architecture," <i>IEEE MICRO</i> , vol. 11, no. 3, June 1991, pp. 10-13 & 63-73.	

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AL	62	Preston et al., "Design of an 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading," in <i>Proceedings of the International Solid State Circuits Conference</i> , January 2002. Slides from talk at conference also referenced, 6 pages total.	
AL	63	Raasch et al., "A Scalable Instruction Queue Using Dependence Chains," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , Anchorage, Alaska, USA: ACM, May 25-29, 2002, 12 pages total.	
AL	64	Rau et al., "Instruction-level parallel processing: History, overview and perspective," <i>International Journal of Supercomputing</i> , vol. 7, pp. 9-50, October 1996.	
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AL	66	Riseman et al., "The Inhibition of Potential Parallelism by Conditional Jumps," <i>IEEE Transactions on Computers</i> , vol. C-21, no. 12, pp. 1405-1411, December 1972.	
AL	67	Rotenberg et al., "Control independence in trace processors," in <i>IEEE Symposium on Microarchitecture</i> , pp. 4-15, December 1999.	
AL	68	Rotenberg et al., "Trace processors," in <i>IEEE Symposium on Microarchitecture</i> , pp. 138-148, December 1997.	
AL	69	Sankaralingam et al., "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," in <i>Proceedings of the 30th Annual International Symposium on Computer Architecture</i> , San Diego, California, USA: ACM and IEEE, June 9-11 2003, 12 pages total.	
AL	70	Sazeides et al., "The Performance Potential of Data Dependence Speculation & Collapsing," in <i>Proceedings of the 29th International Symposium on Microarchitecture (MICRO-29)</i> : IEEE and ACM, December 1996, pp. 238-247.	
AL	71	Sazeides et al., "The predictability of data values," in <i>Proceedings of the 30th International Symposium on Microarchitecture</i> , pp. 248-258, December 1997, 11 pages total.	
AL	72	Seznec et al., "Register Write Specialization Register Read Specialization: A Path to Complexity-Effective Wide-Issue Superscalar Processors," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> , Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
AL	73	Smith et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," in <i>Proceedings of the 17th Annual International Symposium on Computer Architecture</i> , pp. 344-354, IEEE and ACM, May 1990.	
AL	74	Smith, "A Study of Branch Prediction Strategies," in <i>Proceedings of the 8th Annual Symposium on Computer Architecture</i> , pp. 135-148, IEEE and ACM, 1981.	
AL	75	Smith, "Architecture and Applications of the HEP Multiprocessor Computer," <i>Society of Photo-optical Instrumentation Engineers</i> , no. 298, pp. 241-248, 1981.	
AL	76	Sohi et al., "Multiscalar processors," in <i>Proceedings of the International Symposium on Computer Architecture</i> , IEEE and ACM, pp. 414-425, June 1995.	
AL	77	Su et al., "GURPR - A Method for Global Software Pipelining," in <i>Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO-20)</i> , Association of Computing Machinery, pp. 88-96, December 1987.	

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AL	78	Taylor et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," <i>IEEE Micro</i> , vol. 22, no. 2, pp. 25-35, March-April 2002.	
AL	79	Thomton, "Parallel operation in control data 6600," in <i>Proceedings of the AFIPS Fall Joint Computer Conference</i> , pp. 33-40, 1964.	
AL	80	Tjaden et al., "Representation of Concurrency with Ordering Matrices," <i>IEEE Transactions on Computers</i> , vol. C-22, no. 8, pp. 752-761, August 1973.	
AL	81	Tjaden, "Representation and Detection of Concurrency Using Ordering Matrices," Ph. D. Thesis, The Johns Hopkins University, 199 pages total, 1972.	
AL	82	Tomasulo, "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," <i>IBM Journal of Research and Development</i> , vol. 11, no. 1, pp. 25-33, January 1967.	
AL	83	Tubella et al., "Control speculation in multithreaded processors through dynamic loop detection," in <i>Proceedings of the 4th Symposium on High Performance Computer Architecture</i> , pp. 1423, January 1998.	
AL	84	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," in <i>Proceedings of the 22nd Annual International Symposium on Computer Architecture: ACM</i> , June 22-24 1995, pp. 392-403.	
AL	85	Uht et al., "Branch Effect Reduction Techniques," <i>IEEE COMPUTER</i> , vol. 30, no. 5, pp. 71-81, May 1997.	
AL	86	Uht et al., "Disjoint Eager Execution: An Optimal Form of Speculative Execution," in <i>Proceedings of the 28th International Symposium on Microarchitecture, MICRO-28</i> , pp. 313-325, ACM-IEEE, November/December 1995.	
AL	87	Uht et al., "Realizing High IPC Using TimeTagged Resource Flow Computing," in <i>Proceedings of the Euro-Par 2002 Conference, Springer-Verlag Lecture Notes in Computer Science</i> . Paderborn, Germany: ACM, IFIP, August 28, 2002, pp. 490-499. URL: http://www.ele.uri.edu/~uht/papers/Euro-Par2002.ps .	
AL	88	Uht, "A Theory of Reduced and Minimal Procedural Dependencies," <i>IEEE Transactions on Computers</i> , vol. 40, no. 6, pp. 681-692, June 1991. Also appears in the tutorial "Instruction-Level Parallel Processors", Torng, H.C., and Vassiliadis, S., Eds., IEEE Computer Society Press, 1995, pages 171-182.	
AL	89	Uht, "An Efficient Hardware Algorithm to Extract Concurrency From General Purpose Code," in <i>Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences</i> , January 1986, pp. 41-50.	
AL	90	Uht, "Concurrency Extraction via Hardware Methods Executing the Static Instruction Stream," <i>IEEE Transactions on Computers</i> , vol. 41, no. 7, pp. 826-841, July 1992.	
AL	91	Uht, "Hardware Extraction of Low-Level Concurrency from Sequential Instruction Streams," PhD thesis, Electrical and Computer Engineering, Carnegie-Mellon University, Pittsburgh, December 1985, 200 pages.	
AL	92	Uht, "High Performance Memory System for High ILP Microarchitectures," Technical Report 0797-0002, Department of Electrical and Computer Engineering, University of Rhode Island, August 26, 1997. Available via http://ele.uri.edu/~uht , 10 pages total.	

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AL	93	Wallace et al., "Threaded Multiple Path Execution," in <i>25th Annual International Symposium on Computer Architecture</i> : ACM, June 1998, pp. 238-249.	
AL	94	Wenisch et al., "HDLevo - VHDL Modeling of Levo Processor Components," Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, Technical Report 072001-100, July 20, 2001, URL: http://www.ele.uri.edu/~uht/papers/HDLevo.pdf , 36 pages total.	
AL	95	Wu et al., "Compiler Managed Micro-cache Bypassing for High Performance EPIC Processors," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> . Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
AL	96	Xilinx Staff, "Gate Count Capacity Metrics for FPGAs," Xilinx Corp., San Jose, CA, Application Note XAPP 059 (Y. 1.1), February 1, 1997, URL: http://www.xilinx.com/xapp/xapp059.pdf , accessed: June, 2001, 6 pages total.	
AL	97	Zahir et al., "Os and compiler considerations in the design of the ia-64 architecture," in <i>Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pp. 212-221, November 2000.	

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